ABSTRACT

0035 A split gate FET wordline electrode structure and method for forming the same including an improved polysilicon etching process including providing a semiconductor wafer process surface comprising first exposed polysilicon portions and adjacent oxide portions; forming a first oxide layer on the exposed polysilicon portions; blanket depositing a polysilicon layer on the first exposed polysilicon portions and adjacent oxide portions; forming a hardmask layer on the polysilicon layer; carrying out a multi-step reactive ion etching (RIE) process to etch through the hardmask layer and etch through a thickness portion of the polysilicon layer to form second polysilicon portions adjacent the oxide portions having upward protruding outer polysilicon fence portions; contacting the semiconductor wafer process surface with an aqueous HF solution; and, carrying out a downstream plasma etching process to remove polysilicon fence portions.